Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

~~1~~.A method for programming a single-poly electrical programmable read only memory (EPROM) cell, said single-poly EPROM cell comprising a P-channel floating gate transistor on an isolated N-well of a P-type substrate, and an N-channel coupling device, wherein said P-channel floating gate transistor comprises P^+ drain, P^+ source, P channel defined between said P^+ drain and P^+ source, tunnel oxide on said P channel, and doped polysilicon ~~ploysilicon~~ floating gate on said tunnel oxide, and wherein said N-channel coupling device comprises a polysilicon floating electrode that is electrically connected to said doped polysilicon ~~ploysilicon~~ floating gate and is capacitively coupled to a control doped region formed in said P-type substrate, the method comprising:

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grounding said P-type substrate;

grounding said N-well;

biasing said P^+ drain of said P-channel floating gate transistor to a negative voltage;

grounding or floating said P^+ source of said P-channel floating gate transistor; and

applying a positive voltage on said control doped region

so that said positive voltage being coupled to said P-doped ~~ploysilicon~~ polysilicon floating gate, wherein said P channel of said P-channel floating gate transistor is in "OFF" state, and a depletion region and electron-hole pairs are created at a junction between said P^+ drain and said N well, and band-to-band tunneling (BTBT) induced hot electrons will inject into said doped ~~ploysilicon~~ polysilicon floating gate by tunneling through said tunnel oxide.

[c2] 2.The method for programming a single-poly EPROM cell according to claim 1 wherein said positive voltage applied on said control doped region is Vcc.

[c3] 3.The method for programming a single-poly EPROM cell according to claim 2 wherein Vcc = +3.3V.

[c4] 4.The method for programming a single-poly EPROM cell according to claim 1 wherein said positive voltage applied on said control doped region is Vcc~2Vcc.

[c5] 5.The method for programming a single-poly EPROM cell according to claim 1 wherein said negative voltage is —Vcc.

[c6] 6.The method for programming a single-poly EPROM cell according to claim 1 wherein said negative voltage is —3.3V.

[c7] 7.The method for programming a single-poly EPROM cell according to claim 1 wherein a field oxide layer is disposed between said control doped region and said N well.

[c8] 8.The method for programming a single-poly EPROM cell according to claim 1 wherein shallow trench isolation (STI) is disposed between said control doped region and said N well.

[c9] 9.The method for programming a single-poly EPROM cell according to claim 1 wherein said polysilicon floating electrode of said N-channel coupling device is N-type doped polysilicon floating electrode.

[c10] 10.The method for programming a single-poly EPROM cell according to claim 1 wherein said tunnel oxide has a thickness of about 65Å.

[c11] 11.A method for programming a single-poly electrical programmable read only memory (EPROM) cell, said single-poly EPROM cell comprising a P-channel floating gate transistor on an isolated N-well of a P-type substrate, and an N-channel coupling device, wherein said P-channel floating gate transistor comprises P^+ drain, P^+ source, P channel defined between said P^+ drain and P^+ source, tunnel oxide on said P channel, and doped

B Polysilicon

~~ploysilicon~~ floating gate on said tunnel oxide, and wherein said N-channel coupling device comprises a polysilicon floating electrode that is electrically connected to said doped Polysilicon ~~ploysilicon~~ floating gate and is capacitively coupled to a control doped region formed in said P-type substrate, wherein said N-well is isolated from said control doped region, the method comprising:

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grounding said P-type substrate;

grounding said N-well;

applying a negative voltage of —Vcc to said P^+ drain of said P-channel floating gate transistor;

applying a parasitic BJT turn-on voltage to said P^+ source of said P-channel floating gate transistor; and

applying a positive voltage of +Vcc to said control doped region so that said positive voltage of +Vcc being coupled to said doped Polysilicon ~~ploysilicon~~ floating gate.

[c12] 12.The method for programming a single-poly EPROM cell according to claim 11 wherein said parasitic BJT turn-on voltage is a positive voltage that is adequate to turn on a parasitic bipolar junction transistor, wherein said P^+ source acts as an emitter, said P^+ drain acts as an collector, and said N well acts as a base.

[c13] 13.The method for programming a single-poly EPROM cell according to claim 12 wherein when said parasitic bipolar junction transistor is turned on, a large collector-

is applied to the P^+ drain region 126, a well voltage V_{NW} is applied to the N well 120, and a couple voltage $V_{\text{COUPLE}\ \cancel{\text{CPUPLE}}}$ is B applied to the electrically connected N^+ control regions 134 and 136. The P-type silicon substrate 200 is connected to V_{sub}. According to the preferred embodiment, V_{SOURCE} = GROUND or FLOATING, V_{DRAIN} = —Vcc, V_{NW} = GROUND, V_{COUPLE} = Vcc, wherein Vcc is about 3.0V~5V. In a case that Vcc = 3.3V (typical supply voltage for I/O circuit), by way of example, the voltage conditions are: V_{COUPLE} =+3.3V, V_{SOURCE} =0V, V_{DRAIN} =—3.3V, V_{NW} =0V, and V_{sub} =0V.

[0024] Since the N-channel coupling area 130 is much larger than the area of the P-channel floating gate transistor 101, therefore the coupling ratio is approximately equal to 1.0. As a result, the voltage coupled from the N^+ control regions 134 and 136 to the floating polysilicon electrode 132 will be close to 3.3V. Since the floating polysilicon electrode 132 is contiguous with the floating poly gate 122 of the P-channel transistor 101, thus in programming operation, a positive voltage of about 3.3V will be coupled to the floating poly gate 122. Under the above-described voltage conditions, as specifically indicated in Fig.3, the P channel 129 of the transistor 101 is

in "OFF" state, and a depletion region and electron-hole pairs are created at the junction between the P^+ drain 126 and the N well 120, and band-to-band tunneling (BTBT) induced hot electrons will inject into the floating poly gate 122 by tunneling through the tunnel oxide film 128.

[0025] Please refer to Fig.5 and Fig.6. Fig.5 and Fig.6 are schematic cross-sectional diagrams showing another preferred embodiment for programming the single-poly EPROM cell of Fig.1 at low voltages, wherein Fig.5 shows a cross-sectional view of the single-poly EPROM cell taken along line B-B of Fig.1; and Fig.6 shows a cross-sectional view of the single-poly EPROM cell taken along line C-C of Fig.1. In programming operation, likewise, a source voltage V_{SOURCE} is applied to the P^+ source region 124, a drain voltage V_{DRAIN} is applied to the P^+ drain region 126, a well voltage V_{NW} is applied to the N well 120, and a couple B voltage $V^{COUPLE}_{\cancel{CPUPLE}}$ is applied to the electrically connected N^+ control regions 134 and 136. The P-type silicon substrate 200 is connected to V_{sub}. According to this preferred embodiment, $V_{SOURCE} = +V_{BE}$, $V_{DRAIN} = —Vcc$, V_{NW} = GROUND (or $V_{NW} = 0V$), $V_{COUPLE} = Vcc$, wherein Vcc is about 3.0V~5V; V_{BE} is a positive voltage that is larger than 0V. In a case that Vcc = 3.3V (typical supply voltage for I/O cir-